a gate electrode formed above said gate insulation layer, said gate electrode having an upper portion comprised of polysilicon and a lower portion, said upper portion having a plurality of extensions formed thereon, said extensions of said upper portion extending laterally beyond said lower portion of said gate electrode.

REMARKS

Claims 1 and 27 have been amended. Claims 3 and 32 have been cancelled. Thus, claims 1-2, 4-9, 27-31, and 33-34 remain pending in the present application.

In the Office Action, claims 1-2 and 5-8 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Yamaguchi, et al. (U.S. Patent No. 5,144,393). The Examiner's rejections are respectfully traversed.

The present invention is directed to reducing gate delay in a field effect transistor. With regard to independent claim 1, Applicants describe and claim a transistor including a substrate, an active region defined in the substrate, and a gate insulation layer formed above the active region. Applicants further describe and claim a gate electrode formed above the gate insulation layer, the gate electrode having a middle portion located over the active region. The middle portion includes an upper part that has an extension along the gate length direction that decreases from bottom to top of the upper part. The middle portion also has a gate length and a gate height, wherein a cross-sectional area of the gate electrode in a plane defined by the gate length and the gate height of the middle portion exceeds a value obtained by multiplying the gate length by the gate height.

As understood by the undersigned, Yamaguchi is directed to a polysilicon source-drain (PSD) transistor. In particular, the PSD transistor described by Yamaguchi includes a T-shaped

gate electrode formed of crystalline polysilicon. See, *e.g.* Yamaguchi, col. 2, ll. 7-11 and Figure 7. However, as admitted by the Examiner at item 8 on page 5 of the Office Action, Yamaguchi "does not expressly disclose an upper part of said middle portion decreasing from bottom to top." Thus, Applicants respectfully submit that independent claim 1, and claims 2 and 5-8 depending therefrom, are not anticipated by Yamaguchi and request that the Examiner's rejections of these claims under 35 U.S.C. § 102(b) be withdrawn.

Moreover, it is respectfully submitted that claims 1-2 and 5-8 are not obvious over Yamaguchi in view of Choi et al. (U.S. Patent No. 5,621,236). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P.

§ 2142. A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002) (copy attached). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

As understood by the undersigned, Choi is directed to fabricating a gate-to-drain overlapped MOS transistor. The MOS transistor described by Choi is an inverse-T structure that includes a first conductive layer 23 that includes a lower conductive layer 19 made of poly-crystalline silicon and an upper conductive layer 21 made of "fire-resisting" refractory like silicides. Second conductive layers 33, which are isolated from the lower conductive layer 19, are attached to side wells of the upper conductive layer 21. See Choi, col. 2, ll. 16-37 and Figure 2. For example, Choi teaches that the electric characteristics of the MOS transistor are improved by forming the upper conductive layer 21 of tungsten silicide and stacking the upper conductive layer 21 on the lower conductive layer 19 formed of poly-crystalline silicon.

The Examiner alleges at item 8 on page 5 of the Office Action that it would have been obvious to modify the gate extensions of Yamaguchi with the gate extensions disclosed by Choi for the purpose of reducing gate-to-drain capacitance of the device. Applicants respectfully disagree. Choi is concerned with inverse-T gate electrodes and is completely silent with regard to T-shaped gate electrodes. Conversely, Yamaguchi is concerned with T-shaped gate electrodes and is completely silent with regard to inverse-T gate electrodes. Thus, there is simply no teaching or suggestion in the prior art of record to combine the references in the manner

proposed by the Examiner. Accordingly, Applicants respectfully submit that claims 1-2 and 5-8 are not obvious in view of the cited prior art.

In the Office Action, claims 27-31 and 33-34 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Choi. The Examiner's rejections are respectfully traversed.

With particular regard to independent claim 27, Applicants describe and claim a gate electrode formed above a gate insulation layer, said gate electrode having an upper portion comprised of polysilicon and a lower portion. As discussed above, and as admitted by the Examiner in item 10 on page 6 of the Office Action, Choi "does expressly disclose the upper portion of the gate electrode comprising polysilicon." Thus, Applicants respectfully submit that independent claim 27, and claims 28-31 and 33-34 depending therefrom, are not anticipated by Choi and request that the Examiner's rejections of these claims under 35 U.S.C. § 102(b) be withdrawn.

Moreover, it is respectfully submitted that claims 27-31 and 33-34 are not obvious over Choi because Choi expressly teaches away from forming the upper layer of polysilicon, as proposed by the Examiner. In particular, Choi teaches that the electric characteristics of the MOS transistor are improved by forming the upper conductive layer 21 of tungsten silicide and stacking the upper conductive layer 21 on the lower conductive layer 19 formed of poly-crystalline silicon. Accordingly, Applicants respectfully submit that claims 27-31 and 33-34 are not obvious in view of the cited prior art.

In the Office Action, claim 3 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yamaguchi in view of Choi. Claim 3 has been cancelled, rendering the Examiner's rejection moot.

In the Office Action, claims 4 and 9 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yamaguchi. The Examiner's rejections are respectfully traversed. Claims 4 and 9 depend from claim 1 and, for at least the aforementioned reasons, Applicants respectfully submit that claims 4 and 9 are not obvious in view of Yamaguchi and request that the Examiner's rejections be withdrawn.

In the Office Action, claim 32 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Choi. Claim 32 has been cancelled, rendering the Examiner's rejection moot.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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